ABSTRACT OF THE DISCLOSURE

Encoder circuitry for applying a low-density parity check (LDPC) code to information words is disclosed. The encoder circuitry takes advantage of a macro matrix arrangement of the LDPC parity check matrix in which a left-hand portion of the parity check matrix is arranged as an identity macro matrix, each entry of the macro matrix corresponding to a permutation matrix having zero or more circularly shifted diagonals. The encoder circuitry includes a cyclic multiply unit, which includes a circular shift unit for shifting a portion of the information word according to shift values stored in a shift value memory for the matrix entry, and a bitwise exclusive-OR function for combining the shifted entry with accumulated previous values for that matrix entry. Circuitry for solving parity bits for row rank deficient portions of the parity check matrix is also included in the encoder circuitry.